REMARKS

Present Status of the Application

Claims 1-5 and 7-14 are pending of which claims 1 and 7 have been amended in order to more explicitly describe the claimed invention. It is believed that no new matter adds by way of amendments made to claims or otherwise to the application. For at least the foregoing reason, Applicants respectfully submit that claims 1-5 and 7-14 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion of the claim rejection under 35 USC 103

1. The Office Action rejected claims 1, 5, 7 and 11-13under 35 USC 103(a) as being unpatentable over Lan et al. (US-6,034,427, hereinafter Lan).

Applicants respectfully disagree and traverse the above rejections as follows. Applicants would like to point out that Lan substantially fails to show that the bonding pads 224A (of FIG. 2B, 2E, and 2F) which the Office Action deems to be equivalent to the second mounting pads of the claimed invention, are [for electrically contacting] with the corresponding pads of the chip as required by Claims 1 and 7, instead Lan substantially teaches that the bonding pads 224A (as shown in FIGS. 2B, 2E and 2F) are for attaching the bonding wires 227A (please see col. 7, lines 21-22). Accordingly, Applicants respectfully submit that Lan cannot meet independent claims 1 and 7 in this regard.

Further, because Lan substantially teaches that the bonding pads 224A are for attaching to the bonding wires 227A, and therefore the bonding pads 224A cannot possibly be arranged in

central area of the package substrate because the chip is mounted in the central area and the chip is electrically connected with the package substrate via the bonding wires 227A. In other words, the bonding pads 224A of Lan substantially [do occupy significant amount of lateral space on the package substrate] and thereby limiting the overall size of the package substrate.

In other words, since the first and second mounting pads of the claimed invention are designed for attaching with the corresponding bumps of the chip that are mounted on the active surface of the chip, therefore the first and second mounting pads can be arranged in the chip mounting area or the central area so that the area below the chip can be fully utilized and therefore the space occupation by the first and second mounting pads across the lateral surface do not encroach beyond the chip mounting area and can be advantageously utilized allowing further size reduction. Thus the overall size of the package substrate can be further reduced compared to the prior art package structure disclosed by Lan which teach using wire bonding configuration.

Applicants provide an improved substrate structure of Flip Chip package having high reliability. Applicants recognized that because there is no clearance between the bump and the solder mask layer after the bump is attached to the bump pad for the SMD design, and therefore the SMD design is relatively not easy to generate voids, thus the product yield can be improved in the subsequent under-filling process, but however the collapse phenomenon and the bondability between the bump and the mounting pad are poor, and therefore the demand for the coplanarity of the substrate of the flip chip package is relatively rigorously required, and therefore the process tolerance is relatively small. Further, Applicants also recognized that in an NSMD design there is a clearance between the bump and the pad opening, the contact area is

relatively large as it includes the ones on the top and side surfaces, and therefore the collapse phenomenon is relatively good, and the bondability is relatively robust, thus the tolerance for the coplanar error of the substrate of the flip chip package is relatively large. However, in order to avoid the generation of the void in the subsequent under-filling process, the pad opening of the solder mask layer needs to be enlarged properly. As a result, the pitch of the mounting pads needed to be increased to meet this requirement, thus the packaging density becomes lower, and this makes the layout work of the substrate of the flip chip package relatively difficult. In the light of the above, Applicants have designed the bonding pads of a substrate structure of Flip Chip package that reflect all the merits of both the SMD and the NSMD design and least of the demerits thereof. In accordance with the above objects, the present inventors proposes a substrate structure of Flip Chip package comprising at least "a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package, the solder mask layer partially covering a first top surface of the first mounting pads while entirely exposing a second top surface and sidewalls of the second mounting pads, wherein the first mounting pads are disposed at a peripheral region of the substrate and the second mounting pads are disposed at a central region of the substrate, and wherein said first and second mounting pads are for electrically contacting with corresponding bumps of a chip as recited by claim 1 and amended claim 7."

The advantages of the above arrangement of SMD and NSMD mounting pads structure are: firstly, since the top surface and the sidewalls of the second mounting pads that are disposed in the central region are completely exposed, therefore the clearance space between the second

mounting pads in the central region is relatively large and therefore the coplanar tolerance is also relatively large; secondly, since the first mountig pads that are disposed in the peripheral region are essentially a SMD structure, and therefore only a portion of the bumps (254) corresponding to the first mounting pads (214) can attach the top surface (214a) of the first mounting pads 214, and because there is no clearance between the bumps and the solder mask, and therefore there no underfill materials is required to fill this (peripheral) area and thus no voids are formed in this region. And further, since the central region 220 is relatively spacious, and the pitch of the second bonding pad 216 is relatively large, i.e., the pad opening is relatively large, and therefore the underfill material can fill this space without the risk of forming any voids. Therefore the yield can be effectively promoted; and thirdly, because the bumps (254) attach not only the top surface (216a) but also the side surfaces 216b the collapse phenomenon can be relatively insignificant. Therefore, the quality of bump-to-mounting pad attachment is promoted. Accordingly, Applicants provides a substrate structure for a flip-chip package by very cleverly making use of known mounting pads structure within the flip-chip package in a manner to produce a novel substrate structure that has higher tolerance of the coplanar error and at the same the process yield can also effectively promoted.

In other words, because Lan substantially teaches using wire bonding scheme for connecting a chip with the package substrate, accordingly the problems faced by the present inventors, i. e., for attaching the bumps of the chip with the first and the second bonding pads will not occur in Lan's invention. In other words, the Lan patent cannot possibly render the claimed invention obvious to one skilled in the art.

For at least the above reasons, it is therefore submitted that claims 1, 5, 7, 11-13 and 15-16 patently define over Lan and should be allowed. Reconsideration and withdrawal of these rejections is respectfully requested.

2. The Office Action rejected claims 2-4, 8-10 and 14 under 35 USC 103(a) as being unpatentable over Lan in view of Admitted Prior Art (hereinafter APA).

Applicants respectfully disagree and would like to point out that because Lan substantially teaches improvement for using wire bonding scheme for electrically connecting the chip with the package substrate and therefore one skilled in the art will not be motivated to modify the package structure of Lan in a manner suggested by the office action to achieve the claimed invention. Further, the disclosure of the material of the insulative layer and structure thereof, patterned circuit layer and fabrication thereof, still cannot cure the specific deficiencies of Lan.

For at least the reasons as substantially discussed above and therefore Applicants respectfully submit that claims 2-4, 8-10 and 14 also patently define over the prior art of record for the same reasons as set forth above. Reconsideration is respectfully requested.

3. The Office Action rejected claims 4 and 10 under 35 USC 103(a) as being unpatentable over Lan in view of Katchmar et al. (US-6,194,782, hereinafter Katchmar).

Applicants respectfully submit that still Katchmar cannot cure the specific deficiencies of Lan for at least the reasons as substantially discussed above and therefore Applicants respectfully

submit that claims 2-4, 8-10 and 14 also patently define over the prior art of record for the same reasons as set forth above. Reconsideration is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-5 and 7-14 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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